REMARKS

Please reconsider this application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering this application and for the courtesy extended to the Applicant's representatives during the telephone interview on February 22, 2010.

Disposition of the Claims

Claims 4, 16, and 27-36 are now pending in this application. Claims 4, 16, and 27 are independent. The other claims depend, directly or indirectly, from the independent claims.

Amendments to the Claims

Claims 4, 16, and 27 have been amended by way of this reply to clarify the claimed invention. Claims 34-36 have been added. No new matter has been added by these amendments. Support may be found in the original claims and the specification as filed.

Rejection(s) under 35 U.S.C. § 103

Claims 4, 16, and 27-33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,043,672 ("Sugasawara") in view of non-patent literature entitled "iDD pulse response testing applied to complex CMOS ICs" ("Beasley"). For the following reasons, this rejection is respectfully traversed.

MPEP § 706.02(j) provides, "to support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of

the references." Further, in *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727 (2007), the Supreme Court noted that the analysis supporting a rejection under 35 U.S.C. § 103 should be made explicit. Hence, the key to supporting any rejection under § 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious (*see* MPEP §§ 2141, 2142).

As described in the Description of the Related Art of the present specification, conventional fault analysis methods "are costly since these methods require the semiconductor IC to be opened and the chip surface exposed. Moreover, multi-layer wiring and large integration of semiconductor IC's render it difficult to specify fault locations." "A fault analysis method with input output signal response and fault simulation can simulate only a fault of which model is stuck on a single line (0 or 1), so called single-stack-at fault (stuck-at-o or stuck-at-1), but neither a fault stuck on multiple signal line, delay fault, nor fault of short circuit in signal wires. Also, since this fault analysis method can not specify the fault location if the discrepancy between the output value of IC and the expected value is not detected, it cannot guess the fault location of non-logical faults, for example short circuit, where the logic did not become abnormal even with a fault inside the circuit."

Further, "in the fault analysis accompanied by the IDDQ testing and fault simulation, since the IDDQ testing is a method designed to measure a power supply current of semiconductor IC in its stable state and does not have the transient information of the semiconductor IC, it is difficult to specify the fault location altering a delay time of a circuit. Also, because the IDDQ testing, since it is primarily applied to a short defect, cannot detect open defect and abnormality (parametric defects) on local process parameter (sheet resistance, oxidation etc.) causing delay faults, it has been a problem that it could not detect the fault location of delay fault, open defect, and parametric defect." "Therefore, a fault analysis method

is needed that can effectively detect a delay fault and/or open defect and presume the fault location." As such, one or more embodiments of the present invention "provide a method and apparatus which can specify the fault location of a delay fault and/or open defect in a semiconductor IC without processing the semiconductor IC devices." *See* paragraphs [0009] through [0013] of the published specification.

Referring to the specification for purposes of example only, one or more embodiments of the present invention relates to a fault analysis method and apparatus. A test pattern sequence is supplied to a semiconductor IC. An analysis point, whose electric potential changes according to the change of a supplied test pattern, is placed corresponding to the test pattern sequence. Then, a transient power supply current generated on the semiconductor IC, according to the change of the test pattern, is measured. A determination is made as to whether the measured transient power supply current is abnormal or not. A defection point is presumed based on the test pattern sequence where the transient power supply current is abnormal. *See* the Abstract of the published specification. Advantageously, "the reliability of the fault analysis is improved largely because a delay fault or a open defect accompanying a delay fault can be presumed using a method of testing the transient power supply current which is easily observed and having switching information of logic gates." *See* paragraph [0248] of the published specification.

Accordingly, amended independent claim 4 recites, in part, "measuring a time integral of a transient power supply current generated on said semiconductor IC in accordance with the change of said test pattern and determining whether said transient current shows abnormality or not," "presuming a fault location out of said fault location list, based on said test pattern sequence, where the transient power supply current shows abnormality, and said fault

location list," "wherein said presuming comprises: deleting analysis points corresponding to the test pattern sequence where the transient power supply current does not show abnormality from analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality," and "presuming a remaining analysis point out of the analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality to be a fault location," and "wherein the fault location corresponds to at least one of an open defect or a delay fault." Amended independent claims 16 and 27 recite, in part, substantially similar limitations to that of claim 4 noted above.

Sugasawara relates to the "testing of semiconductor devices, and more particularly to selectable power supply lines for use in isolating defects in integrated circuits." *See* column 1, lines 8-10 of Sugasawara. Specifically, Sugasawara discloses that "[d]uring an ATE testing procedure, *the particular section of interest is initially placed in a static test state* in which defects within the section may produce *unusual quiescent current levels*. The selectable power supply line for the particular section is enabled to provide power to the particular section of interest without also powering other sections in the same region of the integrated circuit. By *monitoring quiescent current in the selectable power supply line, areas of unusual quiescent current consumption can be readily identified.* Thus, the use of selectable power supply lines in accordance with the invention permit a failure analysis engineer to significantly reduce defect localization time for an integrated circuit" (emphasis added). *See* column 3, lines 37-49 and column 7, lines 38-53 of Sugasawara.

In the present Office Action, the Examiner alleges that Sugasawara discloses "measuring a time integral of a transient power supply current generated on said semiconductor IC" as required by the independent claims, noting that "[o]nce halted, (i.e. no transistor state

switching is occurring) the power supply of the device under test is measured by the ATE and the resulting value is compared to predetermined reference values or test limits." *See* Office Action of January 14, 2010, at page 3 (quoting Sugasawara at column 2, lines 14-18).

However, Sugasawara discloses that "[w]hen *testing quiescent current* with a functional test set, *the tester is generally halted at predetermined test steps suitable for quiescent current testing*. Once halted (i.e., no transistor state switching is occurring) the power supply of the device under test is measured by the ATE and the resulting value is compared to predetermined reference values or test limits. *Such quiescent current tests* are effective in detecting many faults that would otherwise not be found by other test strategies" (emphasis added). *See* column 2, lines 12-20 of Sugasawara. Further, Sugasawara discloses that "[a]ccurate *quiescent current testing requires that the device under test be in a static DC condition*, with any circuitry that consumes current in the static DC condition, being disabled or accounted for in the test limits. Preferably analog circuitry, input/output pads, and other circuitry not conducive to quiescent current testing are provided with separate, dedicated power supply inputs, so that digital core circuitry can be tested separately" (emphasis added). *See* column 2, lines 30-37 of Sugasawara. As such, Sugasawara merely discloses that circuits tested within the semiconductor IC are electrically isolated by use of selectable power supply lines and execution of the tester is halted for quiescent current testing in the selectable power supply line.

Applicant respectfully asserts that the Examiner has mischaracterized Sugasawara and wrongly equated the quiescent current testing disclosed in Sugasawara to "measuring a time integral of a transient power supply current generated on said semiconductor IC" as required by the independent claims. As noted above, Sugasawara discloses *quiescent current testing* that explicitly requires that the device under test be in a static DC condition. Sugasawara electrically

isolates a circuit within the semiconductor IC to be tested and performs quiescent current testing in the selectable power supply line.

In contrast, the independent claims of the present invention require a measurement of a time integral of a *transient power supply current generated on the semiconductor IC* in accordance with the change of the test pattern. A determination is made as to whether the *transient current* shows abnormality or not. A fault location is presumed out of the fault location list, based on the test pattern sequence, where the transient power supply current shows abnormality, and the fault location list. The presumption includes deleting analysis points that correspond to the test pattern sequence where the transient power supply current does not show abnormality from analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality. The presumption also includes the presumption that a remaining analysis point out of the analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality to be a fault location. The fault location corresponds to at least one of an open defect or a delay fault.

Advantageously, the independent claims measure the transient power supply current that flows at the time of the test pattern change and presumes that locations that change electric potential due to the change of the test patter include fault locations. Because the locations that change electric potential due to the change of a certain test pattern can be simulated, fault locations can be determined without electrically isolating sections in the device under test. As such, Applicant respectfully asserts that Sugasawara fails to show or suggest, at least, the above-noted limitations required by the independent claims. Applicant respectfully asserts that Beasley also fails to show or suggest, at least, the above-noted limitations.

Newly added claims 34-36 require, in part, that "the fault location list includes one or more locations of components which is connected to a common power supply." Applicant respectfully asserts that Sugasawara and Beasley also fail to show or suggest, at least, the above-noted limitation as well.

In view of the above, independent claims 4, 16, and 27 are patentable over Sugasawara and Beasley, whether considered separately or in combination for at least the reasons set forth above. Dependent claims 28-36 are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 02008/071003).

Dated: March 12, 2010

Respectfully submitted,

By_____

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